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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,550	12/05/2003	Ming-Dou Ker	6811954-15U1	8001

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EXAMINER	
NGUYEN, DAO H	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

Office Action Summary	Application No.	Applicant(s)	
	10/727,550	KER ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-25* is/are allowed.

6)☒ Claim(s) *1-15,26 and 27* is/are rejected.

7)☒ Claim(s) *28-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 01/20/2006.

Claims 1-31 are active in this application.

Claim(s) 32-36 has/have been cancelled.

Remarks

2. Applicant's arguments filed on 01/20/2006 have been fully considered, but are not completely persuasive. Particularly, Examiner do/does not agree with Applicant that the doped regions forming the emitter and collector are not well regions. These doped regions are source of N^+ type (or P^+ type) semiconductor which are needed for the flowing of current. (According to Merriam-Webster's Collegiate Dictionary, Tenth Edition, a well is a source from which something may be drawn as needed).

The rejection of the previous Office Action is hereby corrected to better address the teaching of Ker et al. New ground of rejection is/are also included.

Claim Objection

3. In claim 26, a preposition "of" should be inserted between "the collector" and "the first BJT" on the last line of the claim to put the claim in better form.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim(s) 1-4 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,348,724 to Koomen et al.

Regarding claim 1, Koomen discloses a semiconductor device suitable for applications in an electrostatic discharge (ESD) protection circuit, as shown in figs. 2-3, comprising:

a semiconductor substrate 9;

a first well 14&27 formed in the substrate 9;

a second well 26 formed in the substrate 9; and

a first doped region 28 formed in the second well, wherein the first well 14&27, the second well 26, and the first doped region 28 collectively form a parasitic bipolar junction transistor (BJT), and wherein the first well 14&27 is the

collector of the BJT, the second well 26 is the base of the BJT, and the first doped region 28 is the emitter of the BJT. See also col. 3, line 25 to col. 4, line 29.

Regarding claim 2, Koomen discloses the semiconductor device wherein the first well 14&27 is n-type, the second well 26 is p-type, the first doped region 28 is n-type, and the parasitic BJT is an NPN BJT. See fig. 2.

Regarding claim 3, Koomen discloses the semiconductor device wherein the first well is p-type, the second well is n-type, the first doped region is p-type, and the parasitic BJT is a PNP BJT. See col. 6, lines 12.

Regarding claim 4, Koomen discloses the semiconductor device further comprising a second doped region 15 formed in the first well 14&27; and a third doped region 29 formed in the substrate 9, wherein the second doped region 15 and the first well 14&27 are of a same type of conductivity (n-type), and the second doped region 15 is a contact to the first well 14&27, and wherein the third doped region 29 and the second well 26 are of a same type of conductivity (p-type), and the third doped region 29 is a contact to the second well 26. See fig. 2.

6. Claim(s) 1-3, 15, and 26 is/are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,566,715 to Ker et al.

Regarding claim 1, Ker discloses a semiconductor device suitable for applications in an electrostatic discharge (ESD) protection circuit, as shown in figs. 5b, 6, 9, and 11, comprising:

a semiconductor substrate 30;

a first well 36 formed in the substrate 30;

a second well 32 formed in the substrate 30; and

a first doped region 38 formed in the second well 32, wherein the first well 36, the second well 32, and the first doped region 38 collectively form a parasitic bipolar junction transistor (BJT), and wherein the first well 36 is the collector of the BJT, the second well 32 is the base of the BJT, and the first doped region 38 is the emitter of the BJT. See also col. 4, lines 6-64; and col. 6, line 60 to col. 7, line 13, and the above remarks.

Regarding claim 2, Ker discloses the semiconductor device wherein the first well 36 is n-type, the second well 32 is p-type, the first doped region 38 is n-type, and the parasitic BJT is an NPN BJT. See fig. 5b.

Regarding claim 3, Ker discloses the device comprising all claimed limitations. See col. 6, line 60 to col. 7, line 13.

Regarding claim 15, Ker discloses the semiconductor device further comprising a second doped region 40 for receiving a trigger current or a trigger voltage in an ESD event, wherein a portion of the second doped region is formed

in the first well, and another portion of the second doped region is formed in the second well, and wherein the trigger current or the trigger voltage triggers the BJT to discharge the ESD in the ESD event. See figs. 5 and col. 4, line 51 to col. 7, line 9 of Ker.

Regarding claim 26, Ker discloses a semiconductor device suitable for applications in an electrostatic discharge (ESD) protection circuit, as shown in figs. 5b, 6, 9, 11, comprising:

a semiconductor substrate 30;

a first well 38 (the left well) formed in the substrate 30;

a second well 32 formed in the substrate;

a third well 38 (the right well) formed in the substrate 30;

a first doped region 36 (the left doped region) formed in the second well 32; and

a second doped region 36 (the right doped region) formed in the second well 32, wherein the first well 38, the second well 32, and the first doped region 36 collectively form a first parasitic bipolar junction transistor (BJT), and the second well 32, the third well 38, and the second doped region 36 collectively form a second parasitic BJT, and

wherein the first well 38 is the emitter of the first BJT, the third well 38 is the emitter of the second BJT, the second well 32 is the base of both of the first and the second BJTs, the first doped region 36 is the collector of the first BJT;

and the second doped region 36 is the collector of the second BJT. See also the above remarks, and col. 4, line 10 to col. 7, line 25.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim(s) 4-14, and 27 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,566,715 to Ker et al., in view of U.S. Patent No. 5,637,901 to Beigel. et al.

Regarding claim 4, Ker discloses the semiconductor device further comprising:

a contact region (silicide material collector contact region shown by shaded region in the first well or collector 36 (col. 4, lines 38-39)) formed in the first well 44; and

a third doped region 40 formed in the substrate 30,

wherein the contact region is a contact to the first well 36, and

wherein the third doped region 40 and the second well 32 are of a same type of conductivity (p-type), and the third doped region 40 is a contact to the second well 32. See fig. 5b.

Ker teaches that the collector 36 is coupled to pad 60 (fig. 6) via the contact region made by silicide material (col. 4, lines 38-39 and lines 53-56) but not by a second doped region having the same conductivity type as that of the first well or collector 36.

Beigel discloses a semiconductor device for an ESD circuit, as shown in figs. 3, 5, 6, wherein electrical contact(s) to the collector/emitter and/or base is/are made via highly doped layer(s) which correspondingly has/have the same type of conductivity with that of the collector/emitter and base (N^{++} doped layer 26 is formed in, and contacts, the N-type collector 24 (col. 3, lines 22-25); and P^{++} doped layer 36 is formed in, and contacts, the P-type base 32 (col. 3, lines 36-40)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Ker so that the silicide contact regions formed in the collector/emitter, and base regions are replaced by correspondingly highly doped regions of N-type and/or P-type as those of Beigel in order to assure good electrical contacts to the collector/emitter, and base regions. See col. 3, lines 34-40 of Beigel.

Such modification would create a second doped region having the same type of conductivity (n-type) as that of the first well, and contact to the first well.

Regarding claim 5, Ker/Beigel disclose the semiconductor device further comprising an ESD detection circuit 62, wherein the first doped region 38 is connectable to a power supply (VSS), wherein the second doped region (Collector contact) is connectable to a contact pad 60 for receiving an ESD, and wherein the third doped region 40 is connectable to the ESD detection circuit 62 coupled to the contact pad 60 for detecting the ESD. See figs. 5-6 and col. 4, lines 51-57 of Ker.

Regarding claim 6, Ker/Beigel disclose the semiconductor device wherein the ESD detection circuit 62 provides a trigger current to the third doped region 40 in an ESD event, and wherein the trigger current triggers the parasitic BJT to conduct the ESD current from the second doped region to the first doped region or from the first doped region to the second doped region. See col. 4, line 56-64 of Ker.

Regarding claims 7, 8, Ker/Beigel disclose the semiconductor device comprising all claimed limitations. See figs. 5b, 6, 9, 11, and col. 4, line 51 to col. 7, line 9 of Ker.

Regarding claim 9, Ker discloses the semiconductor device further comprising a fourth doped region 46 formed in the second well 32, wherein the fourth doped region 46 and the second well 32 are of a same type of conductivity (p-type), wherein the fourth doped region is also a contact to the second well,

wherein the third doped region 40 and the fourth doped region 46 are spaced apart from each other, and wherein the fourth doped region is connectable to the power supply. See figs. 5b, 6, 9, 11, and col. 4, line 51 to col. 7, line 9.

Regarding claims 10-14, Ker/Beigel disclose the semiconductor device comprising all claimed limitations. See the rejections of claims 4-9/ and figs. 5b, 6, 9, 11, and col. 4, line 10 to col. 7, line 25 of Ker.

Regarding claim 27, Ker discloses the semiconductor device further comprising a third region (silicide material Emitter contact region shown by shaded region in the first well or left emitter 38 (col. 4, lines 38-39)) formed in the substrate, wherein the third region is a contact to the first well (left emitter) 38;

a fourth doped region 40 formed in the second well 32; and

a fifth region (silicide material Emitter contact region shown by shaded region in the first well or right emitter 38 (col. 4, lines 38-39)) formed in the substrate 32, wherein the fifth region is a contact to the third well (right emitter) 38,

wherein the first and second doped regions 36 are connectable to a contact pad for receiving an ESD in an ESD event, the third and fifth regions are connectable to a power supply, and the fourth doped 40 region is connectable to an ESD detection circuit, wherein the ESD detection circuit is coupled to the contact pad for detecting the ESD. See figs. 5b, 6, 9, 11; and col. 4, line 36-64.

Ker teaches that the third and fifth regions are silicide material regions (col. 4, lines 38-39 and lines 53-56) but not doped regions.

Beigel discloses a semiconductor device for an ESD circuit, as shown in figs. 3, 5, 6, wherein electrical contact(s) to the collector/emitter and/or base is/are made via highly doped layer(s) which correspondingly has/have the same type of conductivity with that of the collector/emitter and base (N^{++} doped layer 26 is formed in, and contacts, the N-type collector 24 (col. 3, lines 22-25); and P^{++} doped layer 36 is formed in, and contacts, the P-type base 32 (col. 3, lines 36-40)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Ker so that the silicide contact regions (third and fifth regions) formed in the collector/emitter, regions are replaced by correspondingly highly doped regions of N-type or P-type as those of Beigel in order to assure good electrical contacts to the collector/emitter regions. See col. 3, lines 34-40 of Beigel.

Allowance

9. Claim(s) 16-25 are allowed. The reason for allowance can be found in the previous Office Action.

Allowable Subject Matter

10. Claim(s) 28-31 is/are objected to as being dependent upon a rejected base claim 26, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed semiconductor device (in addition to the other limitations in the claim) wherein a portion of the third doped region is formed in the first well, and another portion of the third doped region is formed in the second well, and wherein a portion of the fifth doped region is formed in the second well, and another portion of the fifth doped region is formed in the third well.

Conclusion

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00

AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
March 13, 2006